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KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
COYER, RYAN D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/910,206	BEUTEN ET AL.	
	Examiner	Art Unit	
	Ryan D. Coyer	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the amendment filed on 4/10/2009 pertaining to Application No. 09/910206. Claims 1-17 are pending, of which Claims 1, 10 and 13 are in independent form.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 10-11, 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,680,620 to Ross hereinafter called Ross.

Per claim 1:

Ross discloses:

A program stored in a computer readable medium, the program performing a method for monitoring an execution of another program that is executable on at least one microprocessor of a micro controller using a debug logic of the micro controller (abstract, "in a microprocessor, a debug facility traps access to a peripheral device.), comprising:

- *causing the debug logic to trigger an exception upon access to an specific address range during a program execution time* (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap

or software exception that is triggered when a specified I/O or memory address accessed" and col. 4 liens 9-11, "Debug registers DR0-DR4 can each hold an I/O or memory address as a breakpoint (an specific address range));

- *causing the at least one microprocessor to configure the debug logic* (col. 4 lines 10-13, "the condition for generating a debug exception in the Pentium microprocessor is specified in the Debug Control Register."), and

- *causing the debug logic to execute an exception routine after the exception is triggered during the program execution time* (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed);

- *wherein the access to the specific address range includes access to an illegal storage area* (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed");

- *wherein the debug logic and its registers* (program 2) *are operated in parallel to the program execution time* (col. 5 lines 33-35, program 2 is another program such as a monitor power down program which is operating in parallel with program 1) *to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, so as to provide an secure stack check without using the program execution time of the microprocessor, wherein the debug logic monitors a program run* (co 3 line 65 to col. 4 line 2, specifically at col. 5 lines 6-12, "the register is

accessed to determine the address which caused the interrupt.", col. 5, lines 25-27, "the interrupt handler routine then continues executing.", Note that the secure stack check is inherently done without using the program execution time of the microprocessor when the debug logic and its register are operated in parallel to the program execution time); wherein the debug logic monitors a program run (col. 4, lines 44-46 “This address is provided by the program desiring the monitoring, e.g., program 2 in FIG. 5A”).

Per claim 2:

The rejection of claim 1 is incorporated and further, Ross discloses:

wherein: the exception corresponds to an interrupt of the execution of the program (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed”).

Per claim 3:

The rejection of claim 1 is incorporated and further, Ross discloses:

wherein: the debug logic is configured during a startup of the micro controller (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed”. Note that the startup of the micro controller is inherently done without startup of microcontroller the breakpoint cannot be specified).

Per claim 4:

The rejection of claim 1 is incorporated, and further, Ross discloses:

resetting the micro controller, starting up the micro controller again, and initializing the program (col. 4, lines 57-62 "After the system is initialized, the system transfers to a monitor mode of operation. During the monitor mode, as indicated by monitor step 108, the breakpoint register is monitored by processor 12 to determine whether the breakpoint has been triggered, as indicated by the address location which is held as the breakpoint value being accessed").

Per claim 5:

The rejection of claim 4 is incorporated, and further, Ross discloses:

storing at least a type of a fault in a memory storing at least a type of a fault in a fault memory before the micro controller is reset and started up again and before the program is initialized (col. 4, lines 50-53 "at callback address step 104, the callback address of the routine to be called is stored within debug (fault) table 106 within memory 36". Note that in computer environment faults are called 'bugs').

Per claim 6:

The rejection of claim 1 is incorporated, and further, Ross discloses:

storing a memory address that was accessed before an occurrence of the fault in the fault memory before the micro controller is reset and started up again and before the program is initialized (col. 4, lines 50-53 "at callback address step 104, the callback

address of the routine to be called is stored within debug (fault) table 106 within memory 36". Note that in computer environment faults are called 'bugs').

Per claim 7:

The rejection of claim 1 is incorporated, and further, Ross discloses:

the debug logic monitors whether the program accesses a preselectable address range of a memory during the program execution time (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed").

Per claim 8:

The rejection of claim 7 is incorporated, and further, Ross discloses:

wherein: the debug logic monitors whether the program accesses an address range of a stack of the micro controller beyond a preselectable maximum stack size during the program execution time (col. 3 line 65 to col. 4 line 2 "application program specifies a breakpoint in the debug register circuit 13. The breakpoint is a trap or software exception that is triggered when a specified I/O or memory address accessed").

Claim 10 is the apparatus (micro controller) claim corresponding to computer readable medium claim 1, and rejected under the same rational set forth in connection with the rejection of claim 1, above, as noted above.

Per claim 11:

The rejection of claim 10 is incorporated, and further, Ross discloses:

the control element corresponds to one of a read-only memory and a flash memory (col. 3 lines 19-21 "Nonvolatile memory 38 is e.g. a read only memory (ROM) which stores microcode including the basic input output system").

Claims 13 and 14 are the apparatus (micro controller) claim corresponding to computer readable medium claims 1 and 2 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1 and 2 respectively, above, as noted above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a)A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ross in view of US Patent No. 6,535,811 to Rowland et al., hereinafter called Rowland.

Per claim 9:

Ross does not explicitly disclose a code sequence of the program, swapped out from a flash memory of the micro controller into a random access memory of the micro controller, in the flash memory.

However, Rowland discloses in an analogous computer system a code sequence of the program, swapped out from a flash memory of the micro controller into a random access memory of the micro controller, in the flash memory (col. 5, lines 23-25 “memory holding the executable code, typically some type of ROM, had to be swapped with a memory having the new executable code "burned in."” and col. 5, lines 27-29 “flash memory 22 comprises a flash EPROM. Thus, executable code for the microcontroller can be rewritten as necessary”).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of swapping the code between memories as taught by Rowland into the method of monitoring the program as taught by Ross. The modification would be obvious because of one of ordinary skill in the art would be motivated to swap the code between flash and RAM memories to read write the data control relationship during engine operation as suggested by Rowland (col. 2, lines 5-9).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ross in view of Admitted Prior Art, hereinafter called APA.

Per claim 12:

The rejection of claim 10 is incorporated, and further, Ross does not explicitly disclose the micro controller is arranged in a motor vehicle.

However, APA discloses in an analogous computer system the micro controller is arranged in a motor vehicle (Applicant's specification, page 2, lines 4-5 "This type of micro controller is, for example, part of a controller for a motor vehicle").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of the micro controller is arranged in a motor vehicle as taught by APA into the method of monitoring the program as taught by Ross. The modification would be obvious because of one of ordinary skill in the art would be motivated to have the micro controller is arranged in a motor vehicle to provide the control of the internal combustion engine, the transmission, the steering assembly, the chassis, etc. as suggested by APA (page 2, lines 1-10).

Allowable Subject Matter

Claims 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments have been fully and carefully considered but are not found to be persuasive. Applicant's arguments will be addressed in turn, below.

Applicant argues:

In contrast, claim 1 of the present application includes the feature of *causing the debug logic to trigger an exception. Claim 1 clearly provides that the debug logic -- and not the processor -- triggers an exception.* Further, the Specification describes the triggering of an exception as "particularly an interrupt of the program execution." (Specification, p. 8, line 28). The Ross reference, however, explicitly states that "[w]hen processor 12 detects [the breakpoint] register being set, then ***processor 12 generates*** *a device access interrupt.*" (Ross, col. 5, lines 1 to 3 (emphasis added)). As to the text at column 4, lines 37 to 56 of the Ross reference, the cited section does not identically disclose (or even suggest) that the debug register circuit of Ross triggers an exception. Thus, Ross makes plain that its processor -- and not its debug register -- triggers an exception. Therefore, Ross does not identically disclose (or even suggest) the feature of *causing the debug logic to trigger an exception,* as provided for in the context of claim 1.

Claim 1 of the present application also includes the feature of *causing the debug logic to execute an exception routine.* Claim 1 clearly provides that the debug logic -- and not the processor -- executes an exception routine. The Ross reference, however, explicitly states that "***processor 12 executes*** *a debug interrupt service routine.*" (Ross, col. 5, lines 64 to 65 (emphasis added)). As to the text at column 4, lines 37 to 56 of Ross, it only refers to "executing an exceptional routine after the exception is triggered", so that it does not disclose that the debug register circuit of Ross executes an exception routine. That is, Ross makes plain that its processor -- and not its debug register -- executes an exception routine. Therefore, Ross does not identically disclose (or even suggest) the feature of *causing the debug logic to execute an exception routine,* as provided for in the context of claim 1.

(Remarks, pg. 8).

Examiner respectfully disagrees. In Ross, the processor implements the debug logic. The claim language makes no explicit recitation of a separation between the 'debug logic' and the 'microprocessor'. Put differently, a processor implementing debug logic, as in Ross, anticipates the instant claim.

Applicant argues:

In stark contrast, Ross does not disclose any such illegal storage area, since it only states that "[t]he address which is set as a ***breakpoint corresponds to the address*** *which is called when access to the device is desired.*" (Ross, col. 4, lines 42 to 44 (emphasis added)). As to the text at column 5, lines 7 to 15 of Ross, it only refers to "accessing to an illegal storage area or protected address", and therefore simply does not identically disclose that the breakpoint of Ross is an illegal storage area. Thus, the breakpoint address of Ross is a valid address of a connected device, and therefore is not an illegal storage area which is either physically not present, lies outside a storage area provided, or is beyond a preselectable maximum stack size, as provided for in the present application and in the context of the claimed subject matter.

(Remarks, pg. 9).

Examiner respectfully disagrees. Ross discloses a 'trap' which is well known in the art as a device used to detect, *inter alia*, improper memory access. (See, e.g., Ross, col. 3 ln. 64). Accordingly, Ross anticipates the instant claim.

Applicant argues:

In stark contrast, Ross explicitly states that "the breakpoint register is ***monitored by processor 12***," and "***processor 12 continues to monitor*** the breakpoint register." (Ross, col. 4, lines 57 to 64 (emphases added)). Further, the "***processor 12 generates*** a device access interrupt," and "***processor 12 executes*** a debug interrupt service routine." (Ross, col. 5, lines 2 to 3, and lines 64 to 65 (emphases added)). As to the text at column 4, lines 57 to 66, and column 5, lines 32 to 47, Ross only refers to "monitoring of the program 1 and program 2 are operating in parallel," and the text at column 3, line 65 to column 4, line 2, column 5, lines 6 to 12, and lines 25 to 27 of Ross only states "that the secure stack check is inherently done without using the program execution time of the microprocessor when the debug logic and its

register are operated in parallel to the program execution time." However, nowhere do these cited sections identically disclose (or even suggest) that the debug registers of Ross are operated in parallel to the program execution time of the processor because, as quoted above, the processor of Ross -- and not its debug register -- performs all the functions. Thus, Ross plainly does not identically disclose (or even suggest) a debug logic operated in parallel to the program execution time, without using the program execution time of the microprocessor.

(Remarks, pg. 9-10).

Examiner respectfully disagrees. Executing a program while simultaneously monitoring said program inherently requires a degree of parallelism. Moreover, as Applicant notes in his remarks, Ross teaches that "the secure stack check is inherently done without using the program execution time of the microprocessor when the debug logic and its register are operated in parallel to the program execution time." (Rem. pg. 9-10). Thus, Ross discloses a method of monitoring a program as claimed.

Applicants remaining arguments are predicated on the validity of the foregoing unpersuasive arguments and, accordingly, are unpersuasive for at least the same reasons.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action, if any. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN D. COYER whose telephone number is (571) 270-5306 and whose fax number is (571) 270-6306. The examiner can normally be reached via phone on Mon-Thurs, 7a-6p. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen, can be reached on (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RYAN D. COYER/
Examiner, Art Unit 2191

/Wei Y Zhen/

Supervisory Patent Examiner, Art Unit 2191